Feb 23, 2005

App Note 3479: DS2154 – Migrating from Revision A2 to D1

This application note describes the procedures for replacing the A2 revision of the DS2154 with the D1 revision of the DS2154. The D1 revision of the DS2154 is a drop-in replacement for the A2 revision of the DS2154. However, it is possible that the user may experience a timing-related issue while replacing the parts. This application note will describe what to do to correct this problem.

Differences Between the Revisions

The DS2154 revision A2 is manufactured using a 0.8µm CMOS process. The DS2154 revision D1 is manufactured using a 0.6µm CMOS process.

For both the A2 and D1 revision of the DS2154, the registers are in a random state on power-up. The user must program all the internal registers to a known state before proper operation can be ensured. This includes setting the test registers to 00h. The most efficient way to perform this initialization is to use a routine to write 0x00 from address 0x00 to 0xFF.

Transmit-Side Timing Diagrams

For reference, the transmit-side timings between TSYNC and frame number, TSYNC and time slot number, and TSYNC and TCLK are shown in the following figures. Note that they are the same for both the A2 and D1 revisions. (Please refer to the DS2154 data sheet for further details.)

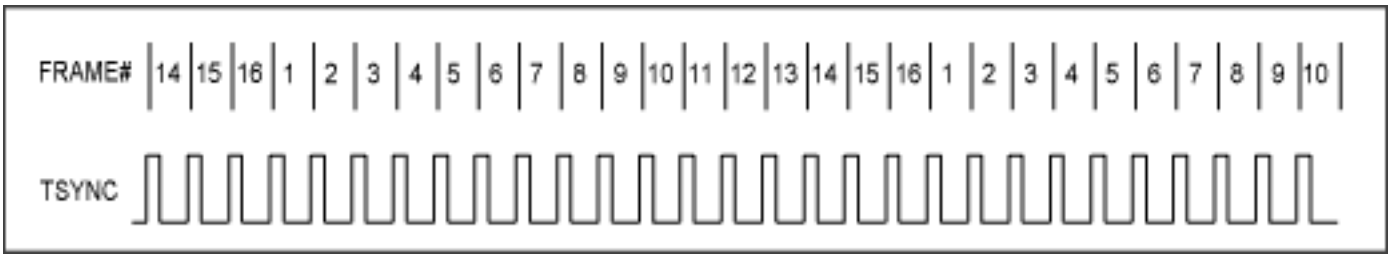

Figure 1. Transmit-Side Timing Between TSYNC and Frame Number

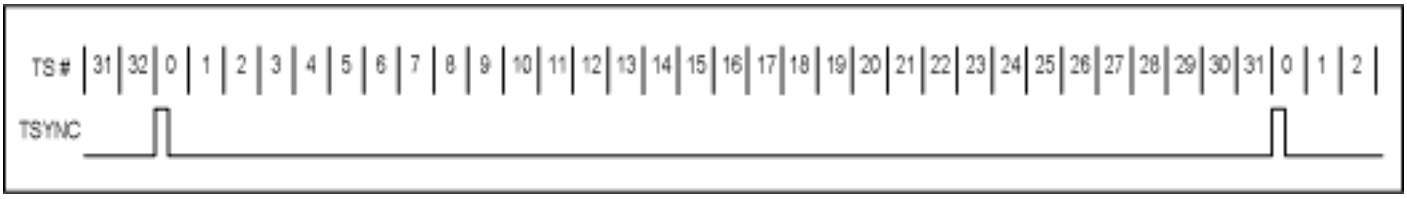

Figure 2. Transmit-Side Timing Between TSYNC and Time Slot (TS) Number

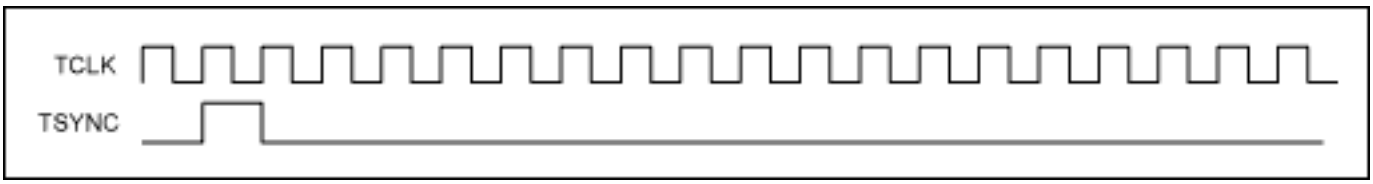

Figure 3. Transmit-Side Timing Between TSYNC and TCLK

In the DS2154 D1 revision, when TSYNC is configured as an input by setting TCR1.0 = 0 (TSIO = 0), the E1 SYNC signal sometimes does not synchronize correctly with the MSB of time slot 0 (TS0). **Figure 4** is the scope image of a possible valid timing diagram between TSYNC and TCLK for the DS2154 A2 revision. However, this is not valid for the DS2154 D1 revision.

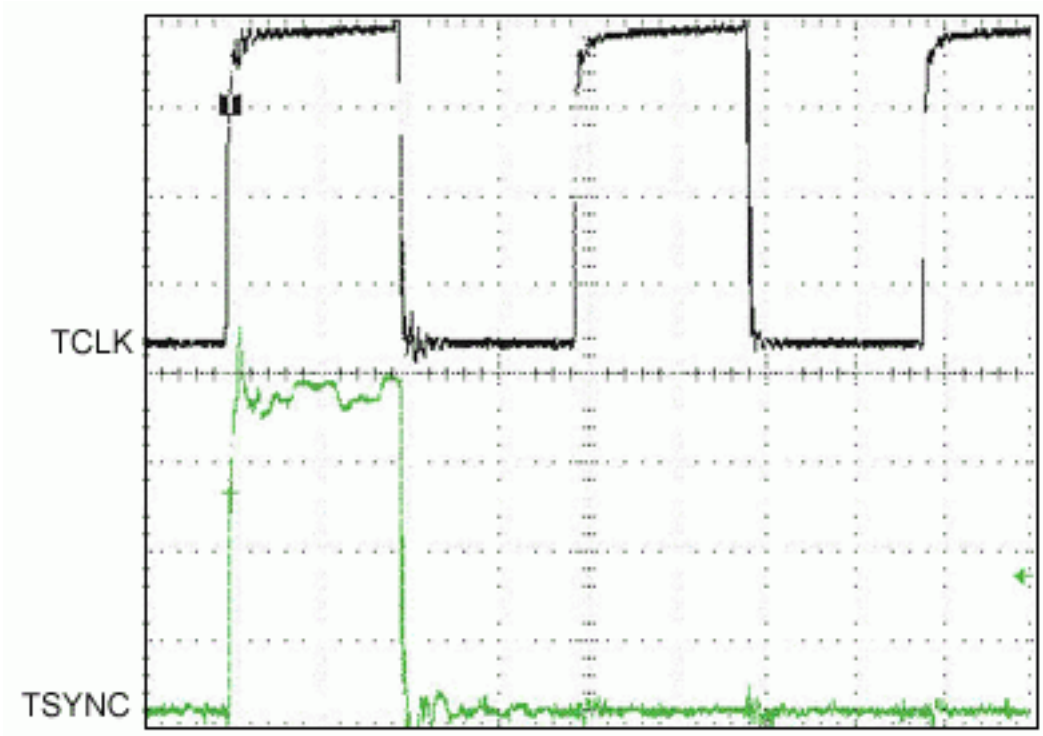

Figure 4. Transmit-Side Timing Between TSYNC and TCLK Taken from an Oscilloscope

Figure 4 shows the falling edge of TCLK and TSYNC as being nearly simultaneous. In the D1 revision, the incoming TSYNC is sampled at the falling edge of TCLK. In order to get the correct sampling, the user needs to add 25ns or more delay onto TSYNC. The user can also make the clock pulse of TSYNC wider. This way, the user can solve the sampling problem. The A2 revison of the DS2154 has a rising edge detector to aid in aligning TSYNC with TS0. The D1 revision of the DS2154 simply samples TSYNC with the falling edge of TCLK. **Figure 5** shows the timing diagram between TCLK and TSYNC after making the TSYNC pulse wider.

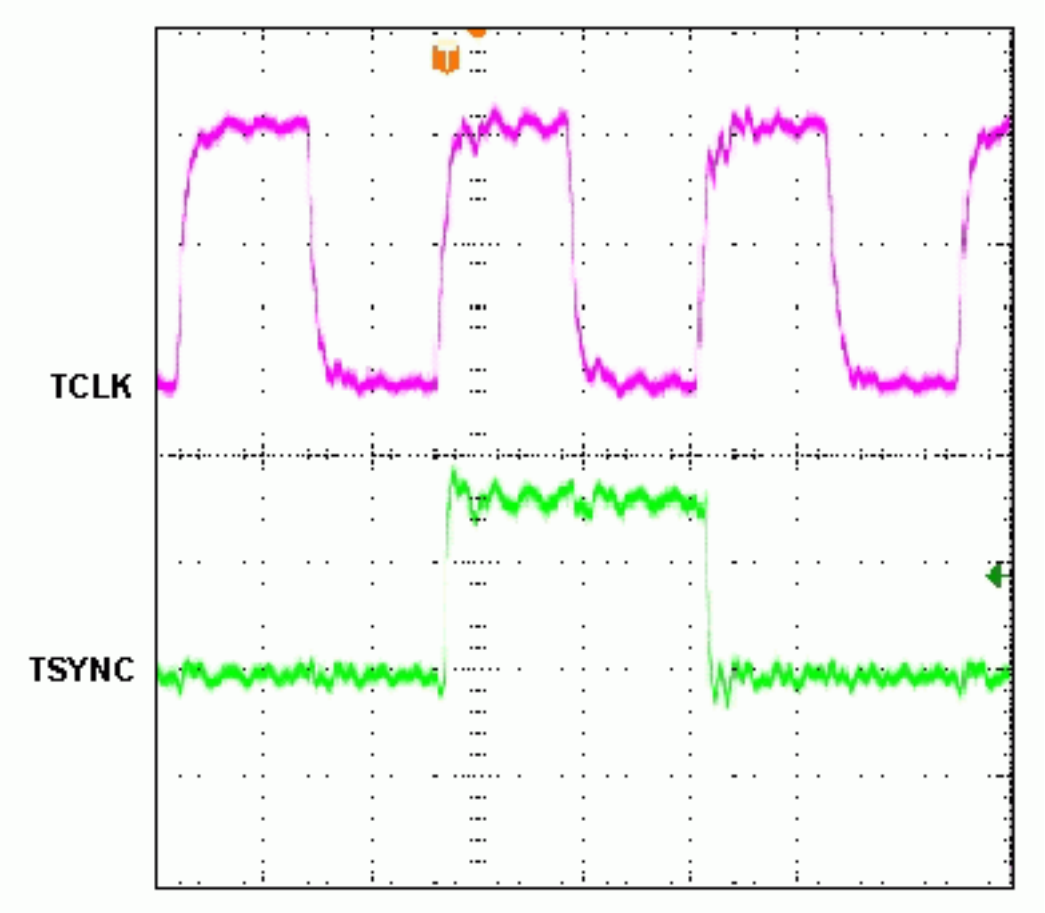

Figure 5. Transmit-Side Timing Between TSYNC and TCLK Taken from an Oscilloscope After Widening the TSYNC Pulse

Conclusion

When replacing the A2 revision of the DS2154 with the D1 revision, most applications will never experience this timing issue. However, if the application experiences this problem, it is recommended to increase the TSYNC delay by 25ns or to widen the TSYNC pulse. For further questions about the operation of the DS2154, please contact the Dallas Semiconductor Telecommunications Applications support team though email: telecom.support@dalsemi.com, or phone: 972-371-6555.

More Information

DS2154: QuickView -- Full (PDF) Data Sheet -- Free Samples